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CCD focal plane array analog image processor

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ABSTRACT

A focal plane array designed for real-time, general-purpose, image preprocessing is described. The analog charge-coupled device-based array operates in the charge domain and has sensing, storing, and computing capabilities. It captures the image data and performs local neighborhood operations. The array is digitally programmable and various image preprocessing tasks can be implemented. It uses a single instruction, multiple data parallel architecture with one processing element serving four pixels. It can be programmed to perform A/D conversion prior to output. The ultra-compact image processor is currently being fabricated with a 3-um, double-poly, double-metal process. The 48 X 48 pixel array is projected to achieve an internal throughput as high as 576 Mops with a 54 dB dynamic range (9-bit equivalent accuracy) and 180 um detector pitch. The total power dissipation is estimated to be 12 mW or less. The total size of the 59-pad chip is 9.4 X 9.4 mm^2.

1. INTRODUCTION

Real-time vision in machines requires the synthesis of imaging hardware, computing hardware, and image processing software. For mobile robots, the system must be portable. These mobile robots may be used in the future for underwater inspection, agriculture, space exploration, and transportation, in addition to obvious defense applications. Thus, the vision system must be lightweight and low-power as well as having the high throughput necessary for achieving real-time operation.

Image preprocessing tasks can be performed using local neighborhood operations on image array picture elements (pixels). Generally, these preprocessing functions consume the greatest portion of time required by the vision process. In the course of effecting the preprocessing tasks, each pixel may undergo as many as 100 to 500 simple arithmetic operations per frame. The frame rate may range from 1 Hz in low speed systems, to 100 Hz in systems operating on a par with human vision, to 1000 to 10,000 Hz in high performance systems. The number of operations required in a 100 Hz frame rate system with a modest array size of 100 X 100 pixels easily could exceed hundreds of Mops (million operations per sec). Advances in very high speed integrated circuits (VHSIC) may allow serial computing systems to achieve such high throughput, but a parallel computing approach can be used to alleviate the performance requirements. Unfortunately, massively parallel computing systems are presently incompatible with the portability

needs of a mobile robot system. Furthermore, the advantages of massively parallel systems often are offset by the problem of loading and unloading the parallel data from a serial data stream at sufficiently high data rates.

It has been proposed to perform the image preprocessing functions in parallel on the image plane itself (Fossum[1] and Joseph et al.[2]). Since the image data arrives in a parallel manner and is transduced to an electrical form in parallel, it seems natural to perform spatially-parallel image preprocessing on the image plane as well. Charge-coupled device (CCD) structures are well-suited for such a system. The analog nature of the image data can be compactly represented in the charge domain, requiring a single electrode for storage. The image data are refreshed at the frame rate, so the dynamic nature of CCD signal representation is generally not a concern. Charge-transfer devices already have established themselves as the technology of choice for image data readout. The difficulty lies in the design of the charge-domain circuits.

In this paper, the design of a CCD focal plane array analog image processor is described. The IRET (in real-time) chip is designed for real-time, general-purpose, image preprocessing. IRET is currently being fabricated and arrangements for testing it are being made. The estimated performance of IRET is described as well.

2. ARRAY ARCHITECTURE

IRET was designed employing a spatially parallel architecture. A detector array of 48 X 48 pixels and a processor array of 24 X 24 processing elements (PEs) are integrated monolithically on IRET. The unit cell of the integrated array consists of one PE and a subarray of 2 X 2 pixels. The PE is a set of various computing and communicating elements and each PE supports 4 pixels. A partial chip layout illustrating the array of the p-n junction photodiode detectors is shown in Fig. 1. The above choices of the sizes of the arrays are of experimental nature and could be generalized to N X N pixels and M X M PEs. The size of the subarray of pixels in the unit cell of the integrated array will be n X n, where n = N/M.

This architecture has two main features. The first one is the integration of the sensing and computing elements in the same cell. This makes the otherwise difficult task of communicating between different elements an easy one. The second main feature is that the array is desiged with a single instruction, multiple data (SIMD) architecture. In this approach, each PE in the array carries out the same instruction, but on a different piece of data depending on the position of the cell in the array. Each PE does not have to be ultra-fast to achieve real-time processing as in the case of serial approaches. A modest clock frequency of 25 MHz and a modest array size of 24 X 24 PEs achieve a total throughput as high as 576 Mops.

The size of the detector subarray supported by each PE, n , is very significant. Increasing n enhances the "fill-factor", the fraction of real estate utilized for photodetection, and improves the spatial

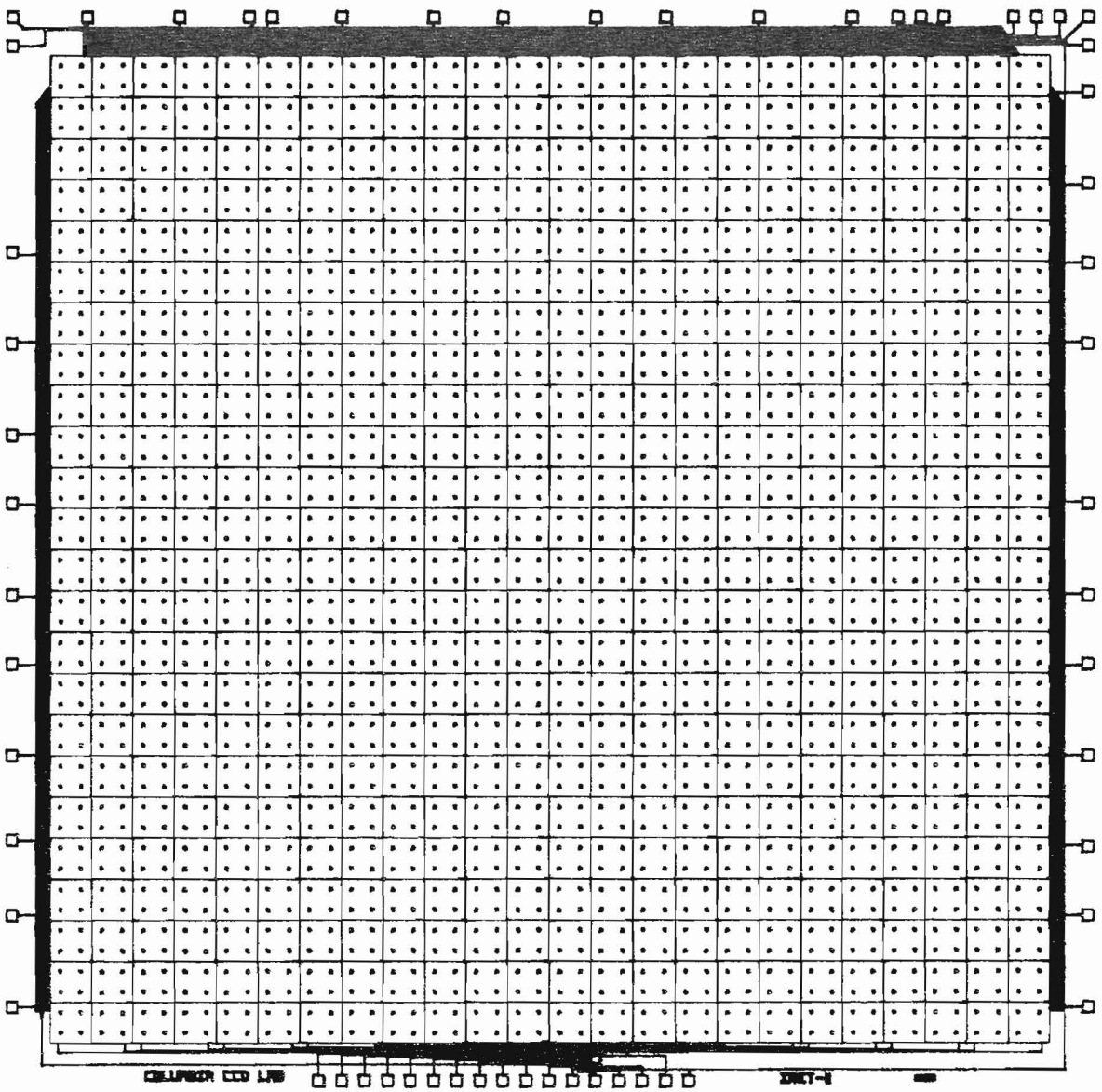

Fig. 1. Chip layout (with unit cell circuitry removed) illustrating the detector array.

resolution of the imager. However, n is limited by the throughput of each PE. A realistic estimate of 1 Mops/PE throughput yields n = 9 with 250 operations per pixel per frame at 50 frames per second. The unit cell size is estimated to be 495 X 495 um^2 with detector pitch of 55 um and detector area 22 X 22 um^2. The choice of n = 2 reduced the complexity of the design and yielded a unit cell size of 360 X 360 um^2 with detector pitch of 180 um and detector area of 22 X 22 um^2. A hybrid or "flip-chip" approach can significantly enhance the fill-factor. The sites of the detectors in Fig. 1 can be viewed as sites for the flip-chip solder bumps.

CCD technology is the heart of this architecture (Fossum[3,4]). The capabilities of CCDs enabled integrating sensing, computing, and storing elements on the same chip. Despite the different functional orientations of these elements, they are all analog and operate in the charge domain. There is no need for A/D or D/A conversion between different stages. CCDs are digitally programmable and so is the array processor. The compactness of CCDs was essential in achieving high density layout. The dynamic nature of CCDs is a key factor in the estimated low power dissipation.

Several tradeoff issues were involved in the design of IRET. Adopting a spatially-parallel architecture eases the speed requirement for real-time processing but intensifies the real estate requirement. A processor array of practical size has to fit on a single chip, thus each unit cell has to be ultra-compact. With n = 9, an array of 250 X 250 pixels (28 X 28 PEs) will yield a chip size of 14 X 14 mm^2. The choice of n = 2 with a 48 X 48 pixel (24 X 24 PE) array size produced a chip size of 9.4 X 9.4 mm^2.

Another tradeoff issue was connectivity. Programming clock signals have to reach each unit cell requiring the accommodation of numerous wires and connections. The requirement of light shielding computing and communicating elements contributed in making the connectivity problem more complex. One layer of metal is devoted to light shielding and the other used for intra-chip wiring. With the help of two layers of polysilicon, wires and connections occupied as much as 60 % of the chip area.

Read-out was another tradeoff issue. Unlike the array processor, the output CCD shift register and amplifier interact with a serial data stream. Real-time read-out requires that the output shift register and amplifier must be M times as fast as the PE. In case of IRET, the output shift register and amplifier operate at 30 MHz.

Power dissipation was also an issue. High numbers of processors operate simultaneously and the total power dissipated by the array must be considered, especially for cooled focal plane arrays. The choice of a CCD technology, which is capacitive in nature, means that the power scales with operating frequency.

3. UNIT CELL ARCHITECTURE

The unit cell has sensing, computing, and communicating circuits.

Each unit cell has a central bus. As shown in Fig. 2, all circuits in the unit cell are connected to the bus through switches. Communication between different elements in the same unit cell is achieved through the bus by applying a sequence of clock signals to the switches. Communication between different unit cells is achieved through a transceiver. The transceiver is a CCD circuit that can be programmed to transceive signals to or from a horizontal, vertical, or diagonal nearest neighbor unit cell. A serial-parallel CCD shift register is used to stack signals coming from the detector subarray. This bidirectional stack can be used for storing purposes.

The unit cell has four CCD computing circuits. Two of them are differencers similar to that reported by Fossum and Barker[5]. One of them is gated by a magnitude comparator similar to that reported by Colbeth et al.[6]. The fourth computing circuit in the unit cell is a splitter similar to that reported by Bencuya and Steckl[7]. Figure 3 shows the layout of the unit cell and Fig. 4 shows the unit cell interconnect architecture.

4. CAPABILITIES

The basic functions of IRET are: capture of the image data, performing local neighborhood operations, and output of a serial data stream that represents the processed image. It performs the local neighborhood operations using basic arithmetic functions such as addition, subtraction, splitting, and magnitude comparison. It also uses conditional addition and subtraction, that is, addition and subtraction conditioned on magnitude comparison.

IRET is a general-purpose image processor. It can be programmed to implement various image preprocessing tasks, each is a convolution of the image data array with a kernel. The kernel has a central element and some surrounding ones. The shape and size of the kernel may differ depending on the nature of the task.

Level shifting and gain adjustments are examples of simple tasks. In the first task the central pixel of the kernel is shifted positively or negatively by a fixed level, while in the second one it is scaled by a fixed fractional factor. Other examples include thresholding or bi-level coding, smoothing or weighted averaging, and sharpening or emphasizing the difference between the central pixel and the surrounding ones. Edge detection is an example of a more sophisticated task that can be implemented.

Another family of image preprocessing tasks is the frame-to-frame set of tasks. Frame-to-frame operations can be performed in a similar manner. An example is a motion detection algorithm which can be implemented using frame-to-frame difference operation.

IRET can be programmed to perform A/D conversion, which is the generalization of bi-level coding. A/D conversion can be performed prior to output. In this case, the output of IRET will be digital.

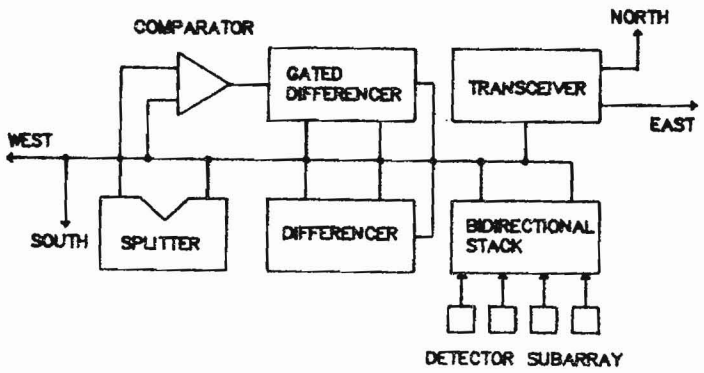

Fig. 2. Block diagram of the unit cell.

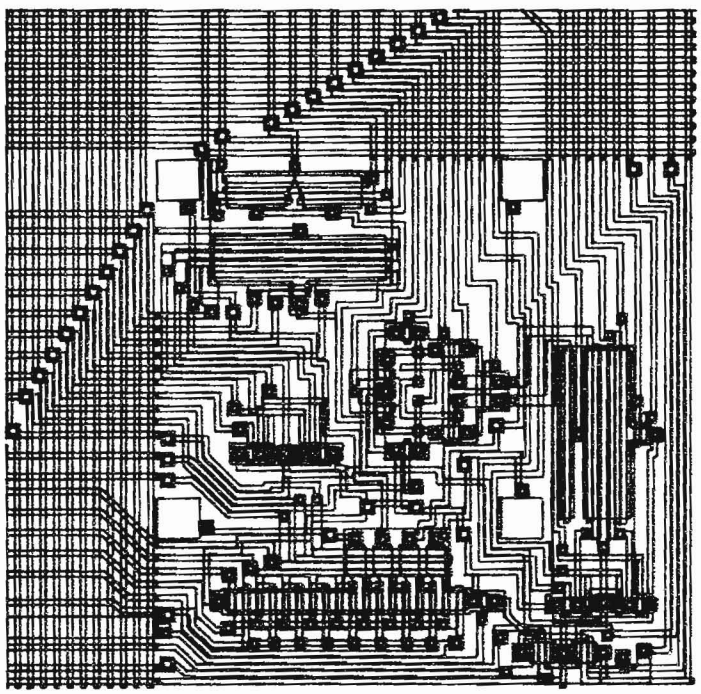

Fig. 3. Layout of the unit cell.

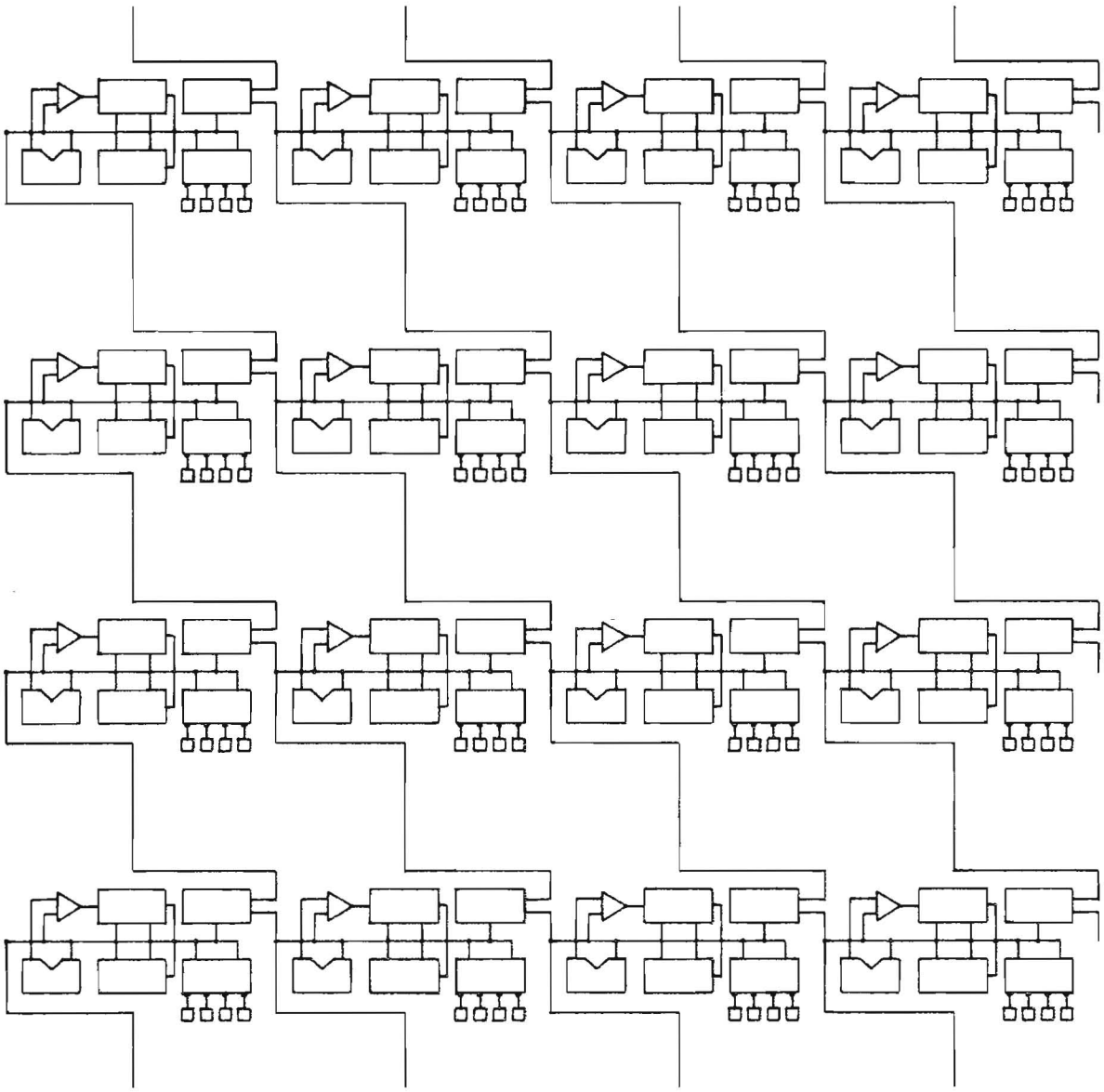

Fig. 4. Unit cell interconnect architecture.

5. PERFORMANCE

IRET is currently being fabricated with a 3-um, double-polysilicon, double-metal process by a commercial CCD foundry service. The prediction of the performance of IRET is based on numerical analysis and experimental results of testing a prototype charge-coupled computer[3]. The assumption that the CCDs will operate with 40 nsec characteristic clock widths is a conservative one. At most, 25 clock cycles are needed to execute any of the basic operations. Thus, the throughput of each PE is estimated to be 1 Mops and the total throughput of the 24 X 24 PE array is estimated to be 576 Mops. On the average, 250 operations per pixel per frame are needed to implement any of the image preprocessing tasks described above. Since each PE supports 4 pixels, 1000 operations per PE per frame are needed. The 1 Mops per PE throughput yields a frame rate of 1000 frames per sec. This frame rate is high and covers a wide range of applications. However, IRET will not operate at this high frame rate because of the relatively limited handling capability of the output shift register and amplifier. It will operate at a nominal frame rate of 50 frames per sec, so the nominal clock frequency will be 1.25 MHz. The total throughput at the nominal point of operation will be 28.8 Mops.

The detectors are expected to have a 60 dB dynamic range (10-bit equivalent accuracy). At 250 operations per pixel per frame, the total noise associated with computation is of the same order of magnitude as the noise associated with sensing the image data (shot noise). Thus, the overall dynamic range is estimated to be 54 dB (9-bit equivalent accuracy).

CCDs are designed to have a maximum signal of one million electrons per pixel. On the average, they are estimated to consume 0.8 pJ per transfer at 10 V clock voltage swing. At the nominal operating point, the clock frequency is 1.25 MHz and the 24 X 24 PEs are expected to dissipate 0.6 mW. At full operation, the clock frequency is 25 MHz and total power dissipation is estimated to be 12 mW.

6. CONCLUSIONS

The design of a CCD focal plane array analog image processor chip (IRET) has been described. The capabilities of IRET to implement various real-time image preprocessing tasks have been theoretically demonstrated and its performance has been predicted. It features high throughput, programmability, compactness, and low power dissipation.

7. ACKNOWLEDGMENTS

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8. REFERENCES

1. E.R. Fossum, Charge-Coupled Analog Computing Elements and Their Application to Smart Image Sensors, Ph.D. thesis, Yale University (1984).

2. J.D. Joseph, P.C.T. Roberts, J.A. Hoschette, B.R. Hanzal, and J.C. Schwanebeck, "A CCD-based parallel analog processor," in State-of-the-Art Imaging Arrays and Their Applications, K.N. Prettyjohns, ed., Proc. SPIE 501, 238-241 (1984).

3. E.R. Fossum, "Charge-coupled computing for focal plane image preprocessing," Opt. Eng. 26(9), 916-922 (1987).

4. E.R. Fossum, "Charge-domain analog signal processing for detector arrays," to be published in Nuclear Instruments and Methods A.

5. E.R. Fossum and R.C. Barker, "A linear and compact charge-coupled charge packet differencer replicator," IEEE Trans. Electron Devices ED-31(12), 1784-1789 (1984).

6. R.E. Colbeth, N.A. Doudoumopoulos, E-S. Eid, S.E. Kemeny, A. Montalvo, and E.R. Fossum, "High performance charge packet comparison for analog CCD applications," Columbia University, CTR Tech. Rep. (1987).

7. S.S. Bencuya and A.J. Steckl, "Charge packet splitting in charge domain devices," IEEE Trans. Electron Devices ED-31(10), 1494-1501 (1984).